ABSTRACT

A method and processor for multiplying two maximally negative fractional numbers to produce a 32-bit result are provided. Operands are fetched from a source location for operation of a multiplication operation. Result outputs corresponding to a maximally negative result are detected. The detection of a maximally negative result indicates that the operands are two maximally negative fractional numbers. Maximally negative results are corrected to produce a maximally positive result. Result output are fractionally aligned and sign extended for accumulation in an accumulator.